What is Claimed is:

1. A fuse formed on an integrated circuit substrate, comprising:

a fuse link that is programmed by applying a programming current; and

at least one heat sink structure, wherein when the programming current is being applied, at least part of the at least one heat sink structure carries heat from the fuse link to the integrated circuit substrate without carrying current.

2. The fuse defined in claim 1 wherein the fuse link comprises polysilicon.

3. The fuse defined in claim 1 wherein the fuse link comprises crystalline silicon.

4. The fuse defined in claim 1 wherein the fuse link comprises crystalline silicon having a p-n junction.

5. The fuse defined in claim 1 wherein the fuse link comprises crystalline silicon having a silicide coating and having a p-n junction.

6. The fuse defined in claim 1 wherein the fuse link comprises polysilicon covered with a layer of material having a lower resistivity than the

polysilicon.

7. The fuse defined in claim 1 wherein the fuse link comprises:

polysilicon; and

a layer of silicide on top of the polysilicon.

8. The fuse defined in claim 1 wherein the fuse link comprises a silicided polysilicon link and wherein the at least one heat sink structure comprises a separate heat sink at either end of the fuse link.

9. The fuse defined in claim 1 wherein the fuse link comprises a silicided polysilicon link and wherein the at least one heat sink structure comprises a separate heat sink at either end of the fuse link and a heat sink at a middle position in the fuse link.

10. The fuse defined in claim 1 wherein the at least one heat sink structure comprises metal that conveys heat from the fuse to the substrate without conducting current.

11. The fuse defined in claim 1 wherein the at least one heat sink structure comprises at least one metal-filled contact hole that conveys heat from the fuse to the substrate without conducting current.

12. The fuse defined in claim 1 wherein the integrated circuit substrate is covered with a dielectric layer having first and second openings and wherein the at least one heat sink structure comprises first and second metal contacts at either end of the fuse link that convey heat from the fuse link to the integrated circuit substrate through the first and second openings.

13. The fuse defined in claim 1 wherein the fuse link comprises polysilicon with a layer of silicide, wherein the layer of silicide has a current-crowding structure that crowds the programming current applied to the fuse link.

14. The fuse defined in claim 1 wherein the fuse link comprises polysilicon with a layer of silicide, wherein the layer of silicide has a notch that narrows the layer of silicide and crowds the programming current being applied to the fuse link during programming.

15. The fuse defined in claim 1 wherein the fuse link comprises polysilicon with a layer of silicide and wherein the fuse link comprises a bend that crowds the programming current being applied to the fuse link during programming.

16. The fuse defined in claim 1 wherein the

fuse link comprises polysilicon having a p-type region and an n-type region that form a p-n junction.

17. The fuse defined in claim 1 wherein the fuse link comprises polysilicon having a p-n junction and a silicide layer having a narrowed portion located at the p-n junction.

18. The fuse defined in claim 1 wherein the at least one heat sink structure helps to blow the fuse at a given position within the fuse link and wherein the fuse link comprises polysilicon having a p-n junction at the given position.

19. The fuse defined in claim 1 wherein the at least one heat sink structure helps to blow the fuse at a given position within the fuse link, wherein the fuse link comprises polysilicon having a p-n junction at the given position, and wherein the fuse further comprises a silicide layer on the polysilicon having a narrowed region that crowds the programming current in the silicide layer during programming.

20. A method of using semiconductor fuses having p-n junctions and conductive thin-film coatings on an integrated circuit, comprising:

applying a programming current to at least some of the fuses, so that some of the fuses are programmed and some of the fuses are unprogrammed; and

using sensing circuitry to determine which fuses have been programmed and to produce corresponding signals for the fuses that indicate whether each fuse has been programmed or is unprogrammed, wherein using the sensing circuitry to determine which fuses have been programmed comprises using both forward-bias and reverse-bias measurements for each fuse to determine whether that fuse behaves ohmically or rectifies.

21. The method defined in claim 20 wherein the sensing circuitry includes storage and wherein using the sensing circuitry to determine which fuses have been programmed comprises:

applying a forward-bias voltage to the fuse;

measuring how much current flows through the fuse as a result of the forward-bias voltage;

storing the measured forward-bias current on the integrated circuit;

applying a reverse-bias voltage to the fuse;

measuring how much current flows through the fuse as a result of the reverse-bias voltage; and

storing the measured reverse-bias current.

22. A fuse on an integrated circuit substrate comprising:

a fuse link having a polysilicon line and a layer of silicide on the polysilicon line, wherein the fuse link has first and second ends; and

first and second metal lines that apply a programming current to the fuse link that flows from the first end of the fuse link to the second end of the fuse link and programs the fuse link by creating an open circuit in the silicide layer, wherein the polysilicon line comprises a p-type doped region and an n-type doped region that form a p-n junction.

23. The fuse defined in claim 22 wherein the first and second metal lines are connected to the first and second ends of the fuse link by metal-filled via holes.

24. The fuse defined in claim 22 wherein the first and second metal lines are connected to the integrated circuit substrate by metal-filed contact holes, so that heat that is generated when the programming current is applied to the fuse link is conveyed from the fuse link to the integrated circuit substrate through the metal-filled contact holes.

25. The fuse defined in claim 22 wherein the first and second metal lines are connected to the integrated circuit substrate by metal-filed contact holes, so that heat that is generated when the programming current is applied to the fuse link is

conveyed from the fuse link to the integrated circuit substrate through the metal-filled contact holes, wherein the integrated circuit substrate has wells of a first doping type in a region of a second doping type that is different from the first doping type, wherein the wells are located where the first and second metal lines are connected to the substrate, and wherein the wells of the first doping type and the region of the second doping type form opposing diodes through the substrate between the first and second metal lines, so that current is not conveyed from the first metal line to the second metal line through the substrate.

26. The fuse defined in claim 22 further comprising a narrowing structure in the silicide layer that crowds the programming current and causes the silicide to form the open circuit in the vicinity of the narrowing structure.

27. The fuse defined in claim 22 further comprising a narrowing structure in the silicide layer that crowds the programming current and causes the silicide to form the open circuit in the vicinity of the narrowing structure, wherein the narrowing structure is located at the p-n junction so that after the fuse has been programmed current applied between the first and second metal lines passes through the p-n junction.

28. The fuse defined in claim 22 further

comprising a notch in the silicide layer that crowds the programming current and causes the silicide to form the open circuit in the vicinity of the notch.

29. The fuse defined in claim 22 further comprising:

a narrowing structure in the silicide layer that crowds the programming current and causes the silicide to form the open circuit in the vicinity of the narrowing structure, wherein the narrowing structure is located at the p-n junction so that after the fuse has been programmed current applied between the first and second metal lines passes through the p-n junction, wherein the first and second metal lines are connected to the integrated circuit substrate by metal-filed contact holes, so that heat that is generated when the programming current is applied to the fuse link is conveyed from the fuse link to the integrated circuit substrate through the metal-filled contact holes, wherein the integrated circuit substrate has wells of a first doping type in a region of a second doping type that is different from the first doping type, wherein the wells are located where the first and second metal lines are connected to the substrate, and wherein the wells of the first doping type and the region of the second doping type form opposing diodes through the substrate between the first and second metal lines, so that current is not conveyed from the first metal line to the second metal line through the substrate.

30. A fuse on an integrated circuit substrate comprising:

a fuse link having a semiconductor line and a thin-film conductive layer on the semiconductor line, wherein the fuse link has first and second ends; and

first and second metal lines that apply a programming current to the fuse link that flows from the first end of the fuse link to the second end of the fuse link and programs the fuse link by creating an open circuit in the thin-film conductive layer, wherein the semiconductor line comprises a p-type doped region and an n-type doped region that form a p-n junction.

31. The fuse defined in claim 30 wherein the semiconductor line comprises crystalline silicon.

32. The fuse defined in claim 30 wherein the semiconductor line comprises polysilicon.

33. The fuse defined in claim 30 wherein the thin-film conductive layer comprises silicide.

34. The fuse defined in claim 30 wherein the semiconductor line comprises crystalline silicon and wherein the thin-film conductive layer comprises silicide.

35. The fuse defined in claim 30 wherein the semiconductor line comprises polysilicon and wherein the thin-film conductive layer comprises silicide.

36. The fuse defined in claim 30 wherein the substrate comprises a silicon-on-insulator substrate having a buried oxide layer that is adjacent to the semiconductor line.